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(71) Applicant *(for all designated States except US)*: VLSI VISION LIMITED [GB/GB]; Technology Transfer Centre, King's Buildings, Mayfield Road, Edinburgh EH9 3JL (GB).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)* : DENYER, Peter, Brian [GB/GB]; 91 Colinton Road, Edinburgh EH10 5DF (GB).

(74) Agents: McCALLUM, William, Potter et al.; Cruikshank and Fairweather, 19 Royal Exchange Square, Glasgow G1 3AE (GB).

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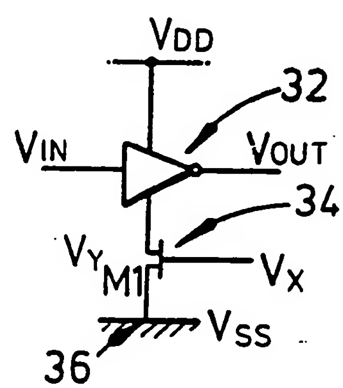

(57) Abstract

The present invention relates to apparatus for minimising the variation in characteristics across different parts of an integrated circuit component (10) caused by manufacturing process variations between a plurality of inverting amplifiers (32) in said component (10). The apparatus comprises at least one transistor (34) connected in series with a power supply terminal (36) on each of the inverting amplifiers (32) so as to provide a new voltage supply reference level for each inverting amplifier (32). By this means the switching threshold of the inverting amplifier (32) is controllable by a voltage (Vx) applied to a control input connection of said transistor (34). Preferably the transistor is a field-effect transistor (34) and the control input connection is to the gate of said transistor (34).

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APPARATUS FOR COMPENSATING MANUFACTURING PROCESS VARIATION

The present invention relates to apparatus for minimising the variation in characteristics of integrated circuit components caused by manufacturing process variations in integrated circuit technology especially MOS technology. In particular, the apparatus may be implemented in a circuit for normalising the switching threshold characteristic of an MOS inverter. Applicants co-pending PCT application No. PCT/GB90/01452 Publication No. WO91/04633, the contents of which are incorporated herein by reference thereto, describes an IC charge sensing circuit in which small quantities of charge which have been integrated at pixel locations are initially detected at charge-sense amplifiers at the top of each column. Under some process conditions a slight deterioration in image quality has been noticed. For example, on a TV screen there is more visible vertical striping. This is believed to be due to process variation affecting mismatch in the column amplifiers.

To achieve a uniform image representation it is therefore necessary to minimise or cancel effects of manufacturing process variation across different parts of the IC circuit, and in particular between the charge sense amplifiers at the top of each column to ensure that these are well matched with each other, in relation to their operating characteristics. The mismatched amplifiers cause the non-uniform vertical striping effect on the detected image. A typical cause of mismatch in such amplifiers is variation in the switching threshold which is caused by threshold or gain variations in its component devices, for example, the inverter used in each of the charge sense amplifiers.

Accordingly, it is an object of the present invention to minimise the manufacturing process variation in component devices and to ensure that the amplifiers based on these component devices are as well matched as possible in order to achieve uniform image representation in applications using solid state image sensors.

It is also an object of the present invention to obviate or mitigate at least one of the disadvantages associated with the existing arrangement.

In one aspect the invention is achieved by providing a circuit which automatically adjusts the switching threshold of the inverters within each amplifier to be close or equal to an externally given voltage so that the amplifier settles at a predetermined operating point.

This is implemented by having at least one transistor in series with at least one power rail connection to the inverting amplifier. The transistor is preferably a field-effect transistor.

In a preferred arrangement three field-effect transistors are used to achieve automatic adjustment of the inverting amplifier switching threshold to approach an external reference voltage. In this arrangement a second transistor couples the output of the inverting amplifier to control the voltage applied to the gate of the first transistor so that the circuit settles to a stable value of voltage such that the switching threshold is achieved at an inverting amplifier external input voltage which is the desired operating point.

According to one aspect of the present invention there is provided apparatus for minimising the variation in

characteristics of integrated circuit components caused by manufacturing process variations, said apparatus comprising at least one transistor connected in series with a power supply terminal of an inverting amplifier, the transistor provides a new voltage supply reference level for the inverting amplifier whereby the switching threshold of the inverting amplifier is controlled by a voltage applied to a control input of said transistor.

In another aspect the present invention provides apparatus for minimising the variation in characteristics across different parts of an integrated circuit component caused by manufacturing process variations between a plurality of inverting amplifiers in said component, which apparatus comprises at least one transistor connected in series with a power supply terminal on each of said inverting amplifiers so as to provide a new voltage supply reference level for each inverting amplifier whereby the switching threshold of the inverting amplifier is controllable by a voltage (Vx) applied to a control input connection of said transistor.

Preferably the transistor is a field-effect transistor and the control input connection is the gate of said transistor. Alternatively the transistor is a bipolar transistor and the control input connection is the base of the transistor.

Preferably the output of the inverting amplifier is coupled to the gate of the field-effect transistor via a second field-effect transistor to provide negative feedback such that the circuit settles to operate at a stable value of gate input voltage for said at least one inverting amplifier.

Preferably also the value of gate input voltage is selected such that the switching threshold of the inverting amplifier is achieved at an externally imposed input voltage to said inverting amplifier to provide the desired operating point for said inverting amplifier.

Advantageously, a gate voltage storage means is coupled to the gate of said at least one transistor such that once the desired operating condition has been reached said second field-effect transistor may be turned-off whereby the correctly adjusted gate input voltage is retained by said voltage storage means whereby the inverting amplifier exhibits a switching threshold approximately equal to said externally imposed voltage.

Conveniently the apparatus for compensating for variation in characteristics of integrated circuit components caused by manufacturing process variations is implemented in a circuit applied to each amplifier in a group of inverting amplifiers to equalise the threshold switching characteristics of each of the inverting amplifiers in the group. This is conveniently done using automatic compensation with a feedback circuit of each column amplifier in a solid state image sensor of the type disclosed in co-pending International Patent Application No. PCT/GB90/01452 Publication No. WO91/04633 for minimising mismatch effects in MOS image sensors.

The manufacturing process variation compensation circuitry may be applied to inverting amplifiers produced by various different manufacturing technologies such as NMOS, CMOS, Bipolar, BiMOS, BiCMOS or GaAs construction.

According to another aspect of the present invention there is provided a method of minimising variations in operating characteristics across different parts of an integrated circuit component caused by manufacturing process variations between a plurality of inverting amplifiers in said component comprising the steps of: providing each inverting amplifier with an additional transistor for normalising the switching threshold characteristic of the inverting amplifier in each of said inverting amplifiers, coupling the transistor in series with at least one power rail connection of the inverting amplifier, and applying a voltage to a control input connection of said transistor to control the switching threshold of said inverting amplifier. Preferably the transistor is a field-effect transistor and the control input connection is the gate of the transistor.

Preferably the method includes the steps of automatically adjusting the inverting amplifier switching threshold to approach a given external reference voltage applied to the inverting amplifier input by feeding the output of the inverting amplifier back to the gate voltage of said field-effect transistor to provide negative feedback and selecting suitable design values for the circuit so that said gate voltage settles to a stable voltage value such that the gate voltage is adjusted to lie within a desired range of the inverting amplifier transfer characteristic whereby the switching threshold is achieved at the inverting amplifier input voltage, which is the desired operating point.

Furthermore, the method includes the step of coupling a voltage storage element in the form of a capacitor in said feedback circuit between the gate and a second

voltage reference level or ground to retain the gate voltage in said capacitor in the event that the feedback loop is broken. Conveniently, the feedback loop includes a second field-effect transistor which is coupled in series between the output connection of the inverting amplifier in the feedback loop and the gate of the first field-effect transistor.

These and other aspects of the present invention will become apparent from the following description when taken in combination with the accompanying drawings in which:-

Fig. 1 depicts the architecture of an array image sensor incorporating a plurality of channel sense amplifiers which require to be matched to achieve uniform image representation;

Fig. 2 is a circuit diagram of an embodiment of the present invention;

Fig. 3 depicts the transfer characteristic of the inverting amplifier shown in Fig. 1 for varying values of drain voltage;

Fig. 4 depicts an alternative embodiment of the present invention which includes negative feedback to achieve automatic adjustment of the inverting amplifier switching threshold to meet that of an externally imposed voltage; and

Fig. 5 depicts a further embodiment of a process variation compensation circuit for use with an inverting amplifier implemented in CMOS technology.

Reference is first made to Fig. 1 of the drawings which

depicts an array image sensor generally indicated by reference 10 which consists of an array of pixels 12 laid out in generally rectangular format in rows and columns. Each pixel 12 in a row is connected to a common horizontal line called a word-line 14 and each word line is connected to digital circuitry 16 which is used to generate and drive the necessary pattern of word line signals. This circuitry 16 generally takes the form of a shift register. Each vertical column of pixels is connected to a common conductor known as a bit-line 18 which is connected to a respective analogue switch sense amplifier circuit 20.

The amplifier 20 has two inputs 19,21 and one output 22. The input 21 coupled to a common digital circuit 24 which produces enabling signals that control the analogue or sense amplifier circuits 20 to enable the signals on consecutive bit-lines to be connected to the output of the array image sensor 10. Conveniently the digital circuitry 24 is realised by a shift register. The output of each amplifier 20 is connected to a common conductor 26 which functions as a common read out line and which is connected to a sense amplifier 28. The amplifier 28 has an output 30 from which the output of the integrated circuit is taken.

Reference is now made to Fig. 2 of the drawings which depicts a circuit for automatically adjusting the switching threshold of an inverting amplifier 32 to be close or equal to an externally given voltage. The circuit shown in Fig. 1 is for the case of an arbitrary inverting amplifier. At least one field-effect transistor 34 is connected in series with at least one power rail (ground) connection 36 of the inverting amplifier 32. The field-effect transistor 34 is an n-channel MOS transistor M1 connected in series with the

ground power connection VSS of the inverting amplifier.

The drain voltage V_y of transistor 34 effectively becomes the new ground reference for the inverting amplifier 32. Accordingly, it will be appreciated that the transfer characteristic of the inverting amplifier is dependent on the V_y and generally the switching threshold of the inverting amplifier varies in a proportional relationship to V_y as best seen in Fig. 3. It will be understood that V_y is determined by the inverting amplifier supply current and also the channel resistance of field-effect transistor 34. The channel resistance of the field-effect transistor 34 is, in turn, determined by the gate voltage, designated as V_x. Therefore, it will be understood that the switching threshold of the inverting amplifier 32 is controlled and adjusted by varying the gate voltage V_x on the transistor 34.

Reference is now made to Fig. 4 of the drawings which depicts an alternative embodiment of a manufacturing process variation compensation circuit used with an inverting amplifier 32 to provide automatic adjustment of the inverting amplifier switching threshold to approach a given external reference voltage designated as V_b. The external reference voltage V_b is applied to the inverting amplifier input 38 as shown in Fig. 3b via a field-effect transistor generally indicated by reference numeral 40. A third field-effect transistor 42 is connected in the feedback path between the output of the inverting amplifier 44 and the gate 46 of transistor 34. This is a configuration of negative feedback and for suitable design values the process variation compensation circuit settles to a stable value of V_x. It is possible to further select design values such that the value of V_x normally lies within the high

gain portion of the inverting amplifier transfer characteristic as shown in Fig. 3. This is the desired operating point of the amplifier. Once the desired operating point has been reached the transistor 42 can be turned off thereby breaking the feedback loop. However, a capacitor 48 coupled between the gate of transistor 46 and ground stores the correctly adjusted value of V_x on the capacitor 48. In this case the inverting amplifier may now be used in its normal capacity and exhibits a switching threshold which is approximately equal to the external reference voltage input V_b.

In practice, it will be appreciated that second-order effects such as non-infinite inverting amplifier gain limit the accuracy of the adjusting switching threshold, but in a practical application using a CMOS inverting amplifier this circuit is found to compensate by about a factor of 30 for switching threshold offsets amongst a group of inverting amplifiers.

Reference is now made to Fig. 5 of the drawings in which the inverting amplifier 44 is implemented by a CMOS inverting amplifier, generally indicated by reference numeral 52, otherwise the circuit components are identical to those shown in Fig. 4.

It will be appreciated that various modifications may be made to the circuits hereinbefore described without departing from the scope of the invention. For example, the circuit may also be implemented by connecting a field-effect transistor or the like in series with the positive supply rail or by a combination of transistors connected in series with both supply rails. Bipolar transistors may be used with the control input being applied to the base of the transistor. It will be

appreciated that the circuitry hereinbefore described may be implemented in a range of different technologies such as NMOS, CMOS, Bipolar, BiMOS, BiCMOS or GaAs construction.

It will be appreciated that the principal advantage of this invention is that variations in characteristics of i.c. amplifiers because of manufacturing process variations resulting in amplifier mismatch is compensated automatically so that the inverting amplifier switching threshold is set to a given external reference voltage. This results in minimising the switching threshold offsets by about a factor of 30 amongst a group of inverting amplifiers such as in a row of channel sense amplifiers shown in fig. 1, greatly improving uniform image representation in applications using solid state MOS image sensors.

CLAIMS

1. Apparatus for minimising the variation in characteristics across different parts of an integrated circuit component (10) caused by manufacturing process variations between a plurality of inverting amplifiers (32) in said component (10), which apparatus comprises at least one transistor (34) connected in series with a power supply terminal (36) on each of said inverting amplifiers (32) so as to provide a new voltage supply reference level for each inverting amplifier (32) whereby the switching threshold of the inverting amplifier (32) is controllable by a voltage (Vx) applied to a control input connection of said transistor (34).

2. Apparatus according to claim 1 wherein the transistor is a field-effect transistor (34) and the control input connection is to the gate of said transistor (34).

3. Apparatus according to claim 1 wherein the transistor is a bipolar transistor and the control input connection is to the base of the transistor.

4. Apparatus according to claim 2 wherein the output of the inverting amplifier (44) is coupled to the gate of the field-effect transistor (46) via a second field-effect transistor (42) to provide negative feedback such that the circuit settles to operate at a stable value of gate input voltage for said inverting amplifier (44).

5. Apparatus according to claim 4 which is formed and arranged so as to apply a gate input voltage having a value selected such that the switching threshold of the inverting amplifier (44) is achieved at an externally

imposed input voltage to said inverting amplifier (44) to provide a desired operating point for said inverting amplifier (44).

6. Apparatus according to claim 2, claim 4 or claim 5, wherein is provided a gate voltage storage means (48) coupled to the gate of said at least one transistor (46) such that once the desired operating point has been reached said second field-effect transistor (42) may be turned-off whereby the correctly adjusted gate input voltage (Vx) is retained by said voltage storage means (48) whereby the inverting amplifier (44) exhibits a switching threshold approximately equal to said externally imposed voltage.

7. An integrated circuit component (10) comprising a plurality of inverting amplifiers (32) wherein at least some of said inverting amplifiers (32) are provided with compensating apparatus (34) according to any one of the preceding claims, so as to equalise the switching threshold of the inverting amplifiers (32) in the group consisting of said at least some inverting amplifiers (32).

8. A integrated circuit component (10) according to claim 7 which component (10) comprises a solid state image sensor (2).

9. A method of minimising variations in operating characteristics across different parts of an integrated circuit component caused by manufacturing process variations between a plurality of inverting amplifiers in said component comprising the steps of:
providing each inverting amplifier (32) with an additional transistor (34) for normalising the switching threshold characteristic of the inverting amplifier (32)

in each of said inverting amplifiers (32), coupling the transistor (34) in series with at least one power rail connection of the inverting amplifier (32), and applying a voltage to a control input connection of said transistor (34) to control the switching threshold of said inverting amplifier.

10. A method according to claim 9 wherein the transistor is a field-effect transistor (34) and the control input connection is the gate (33) of said transistor (34).

11. A method according to any one of claims 8 to 10, which method includes the steps of automatically adjusting the inverting amplifier switching threshold to approach a given external reference voltage applied to the inverting amplifier (32) input by feeding the output of the inverting amplifier (32) back to the gate voltage of said field-effect transistor (34) to provide negative feedback and selecting suitable design values for the circuit so that said gate voltage settles to a stable voltage value such that the gate voltage is adjusted to lie within a desired range of the inverting amplifier transfer characteristic whereby the switching threshold is achieved at the inverting amplifier input voltage, which is the desired operating point.

12. A method according to claim 11 which method includes the step of coupling a voltage storage element in the form of a capacitor (48) in said feedback circuit between the gate (33) and a second voltage reference level or ground to retain the gate voltae (Vx) in said capacitor (48) in the event that the feedback loop is broken.

13. A method according to claim 12 wherein is included in the feedback loop a second field-effect transistor (42) which is coupled in series between the output connection (44) of the inverting amplifier (38) in the feedback loop and the gate of the first field-effect transistor (46).

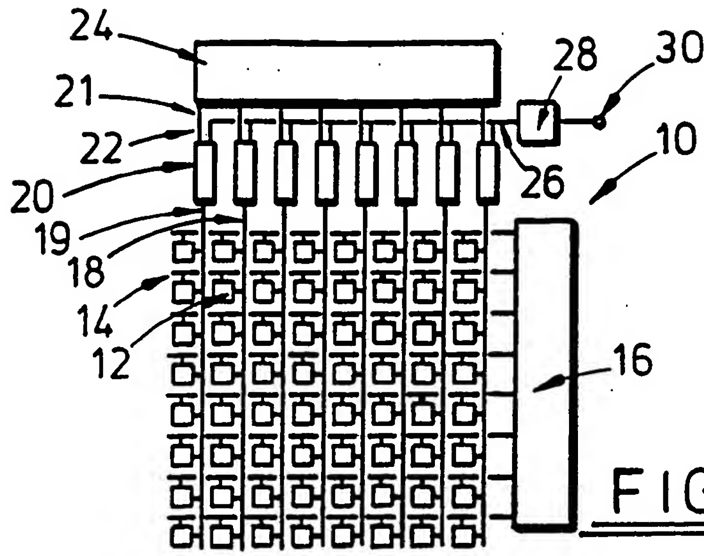

FIG. 1

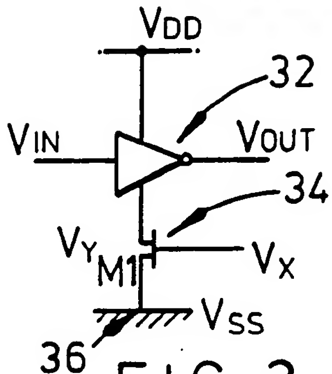

FIG. 2

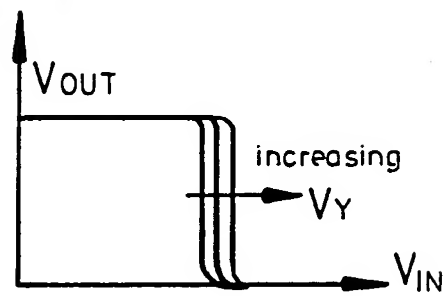

FIG. 3

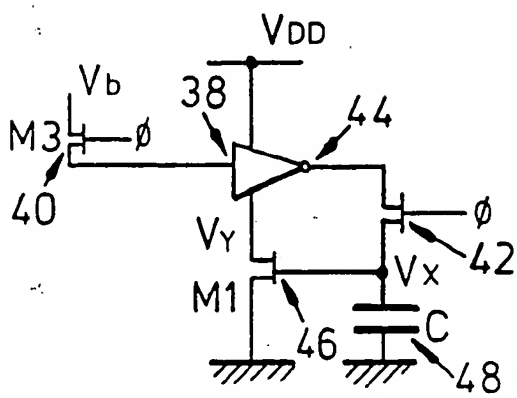

FIG. 4

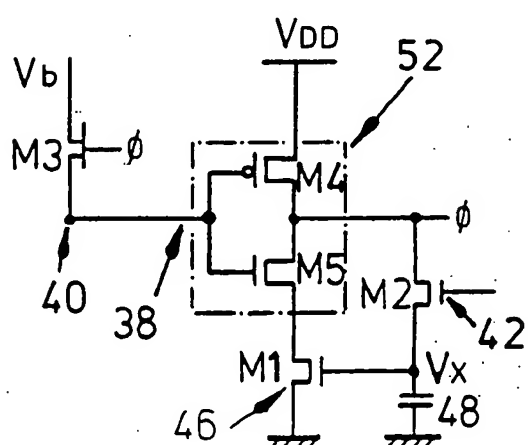

FIG. 5

International Application No

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.Cl. 5 H03K19/00; H03K19/003

II. FIELDS SEARCHED

Minimum Documentation Searched[7]

Classification System	Classification Symbols
Int.Cl. 5	H03K ; H03F

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched[8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

Category °	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No.[13]
Y	PATENT ABSTRACTS OF JAPAN vol. 13, no. 97 (E-723)(3445) 7 March 1989 & JP,A,63 272 120 (FUJITSU LTD) 9 November 1988 see abstract	1-3,9,10
Y	EP,A,0 412 567 (SIEMENS) 13 February 1991 see the whole document	1-3,9,10
Y	EP,A,0 239 844 (SIEMENS) 7 October 1987 see page 7, line 20 - page 8, line 28; figure 3	1-7,9-13
Y	EP,A,0 161 215 (CENTRE ELECTRONIQUE HORLOGER) 13 November 1985 see page 6, line 26 - page 9, line 34; figures 2,4-6	1-7,9-13
A	US,A,4 580 103 (TOMPSETT) 1 April 1986	

° Special categories of cited documents : [10]

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
12 JUNE 1992	24. 06. 92
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	FEUER F.S.

1

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO. GB 9200452
SA 57498

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report.
The members are as contained in the European Patent Office EDP file on 12/06/92
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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP-A-0412567	13-02-91	JP-A- 3076419	02-04-91
EP-A-0239844	07-10-87	CA-A- 1280482	19-02-91
		JP-A- 62220018	28-09-87
		LU-A- 86638	02-04-87
		US-A- 4837778	06-06-89
EP-A-0161215	13-11-85	CH-A- 658349	31-10-86
		DE-A- 3583883	02-10-91
		JP-A- 60239110	28-11-85
		US-A- 4628274	09-12-86
US-A-4580103	01-04-86	None	

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